In the claims

Please cancel and amend the claims as follows:

1. (Currently amended) A method for fabricating a semiconductor device, comprising the steps of:

a) forming a stack layer of a gate layer, a poly-silicon layer, a tungsten layer, and a hard mask sequentially deposited on a semiconductor substrate;

b) carrying out a selective oxidation process, wherein the poly-silicon layer of the stack layer is only oxidized;

c) performing a heat treatment process in a low pressure chemical vapor deposition (LPCVD) furnace for releasing a stress exerted during the selective oxidation process; and

d) carrying out a process for forming a gate sealing nitride layer on the heat treated stack layer.

2. (Original) The method as recited in claim 1, wherein the heat treatment process and the gate sealing nitride layer formation process are carried out by using a low pressure chemical vapor deposition (LPCVD) furnace under an in-situ method.

3. (Original) The method as recited in claim 2, wherein the in-situ method includes the steps of:

a1) loading the semiconductor substrate at which the selective oxidation process is carried out in the LPCVD furnace;

b1) carrying out the heat treatment process by slowly increasing a temperature of the LPCVD furnace from a room temperature to a target temperature for the heat treatment process and keeping the target temperature in a vacuum ambient;

c1) depositing the gate sealing nitride layer after slowly decreasing the temperature of the LPCVD furnace from the target temperature for the heat treatment process to a target temperature for depositing the gate sealing nitride layer; and

d1) unloading the semiconductor substrate after decreasing the temperature of the LPCVD furnace to a room temperature.

4. (Original) The method as recited in claim 3, wherein the target temperature for the heat treatment process ranges from about 750 °C to about 1000 °C and a pressure of the vacuum ambient ranges from about 10^{-3} torr to about 10^{-2} torr.

5. (Original) The method as recited in claim 3, wherein a rising rate of the temperature for the heat treatment process ranges from about 3 °C /min to about 25 °C /min.

6. (Original) The method as recited in claim 3, wherein a falling rate of the temperature for depositing the gate sealing nitride layer ranges from about 1 °C /min to about 20 °C /min.

7. (Original) The method as recited in claim 3, wherein the heat treatment process is carried out for about 10 minutes to about 240 minutes.

8. (Original) The method as recited in claim 1, wherein the heat treatment process and the gate sealing nitride layer formation process carried out in the same LPCVD furnace or two different LPCVD furnaces under the ex-situ method.

9. (Original) The method as recited in claim 8, wherein the ex-situ method includes the steps of:

a2) loading the semiconductor substrate at which the selective oxidation process is carried out in a first low pressure chemical vapor deposition (LPCVD) furnace;

b2) performing the heat treatment process by slowly increasing a temperature of the first LPCVD furnace from a room temperature to a target temperature for the heat treatment process and keeping the target temperature in a vacuum ambient;

c2) unloading the semiconductor substrate after decreasing the temperature of the LPCVD furnace to a room temperature; and

d2) depositing the gate sealing nitride layer after loading the unloaded semiconductor substrate in the first LPCVD furnace or a second LPCVD furnace.

10 (Original) The method as recited in claim 9, wherein the target temperature for the heat treatment process ranges from about 750 °C to about 1000 °C and a pressure of the vacuum ambient ranges from about 10^{-3} torr to about 10^{-2} torr.

11. (Original) The method as recited in claim 9, wherein a rising rate of the temperature for the heat treatment process ranges from about 3 °C /min to about 25 °C /min.

12. (Original) The method as recited in claim 9, wherein a falling rate of the temperature for depositing the gate sealing nitride layer ranges from about 1 °C /min to about 20 °C /min.

13. (Original) The method as recited in claim 9, wherein the heat treatment process is carried out for about 10 minutes to about 240 minutes.

14. (Currently amended) A method for fabricating a semiconductor device, comprising the steps of:

a3) forming a stack layer of a gate oxide layer, a poly-silicon layer, a tungsten layer, and a hard mask sequentially deposited on a semiconductor substrate;

b3) carrying out a selective oxidation process, wherein the poly-silicon layer of the stack layer is only oxidized;

c3) depositing a gate sealing nitride layer on the stack layer selectively oxidized; and

d3) performing a heat treatment process <u>in an LPCVD furnace</u> for releasing a stress

exerted during the selective oxidation process and gate sealing nitride layer deposition process.

15. (Currently amended) The method as recited in claim 14, wherein ~~the selective oxidation process~~ the gate sealing nitride layer deposition process and the heat treatment process are carried out in the identical furnace or in two different LPCVD furnaces under an ex-situ method.

16. (Original) The method as recited in claim 15, wherein the ex-situ method includes the steps of:

a4) depositing the gate sealing nitride layer on the semiconductor substrate in a first low pressure chemical vapor deposition (LPCVD) furnace;

b4) loading the semiconductor substrate on which the gate sealing nitride layer is deposited in a second LPCVD furnace;

c4) performing the heat treatment process by slowly increasing a temperature of the second LPCVD furnace from a room temperature to a target temperature for the heat treatment process and maintaining the target temperature in a vacuum or inert gas ambient; and

c5) unloading the semiconductor substrate after decreasing the temperature of the second LPCVD furnace from the target temperature for the heat treatment to a room temperature.

17. (Original) The method as recited in claim 15, wherein the ex-situ method includes the steps of:

a6) depositing the gate sealing nitride layer in the LPCVD furnace;

b6) loading the semiconductor substrate on which the gate sealing nitride layer is deposited in an annealing furnace used for the heat treatment process;

c6) carrying out the heat treatment process by increasing a temperature of the annealing furnace from a room temperature to a target temperature for the heat treatment

process and maintaining the target temperature in a vacuum or inert gas ambient; and

d6) unloading the semiconductor substrate after decreasing the temperature of the annealing furnace.

18. (Original) The method as recited in claim 16, wherein the temperature for the heat treatment process ranges from about 750 °C to about 1000 °C and a pressure of the vacuum ambient ranges from about 10^{-3} torr to about 10^{-2} torr.

19. (Original) The method as recited in claim 16, wherein a rising rate of the temperature for the heat treatment process ranges from about 3 °C /min to about 25 °C /min.

20. (Original) The method as recited in claim 16, wherein a falling rate of the temperature for the heat treatment process ranges from about 1 °C /min to about 20 °C /min.

21. (Original) The method as recited in claim 17, wherein the temperature for the heat treatment process ranges from about 750 °C to about 1000 °C and a pressure of the vacuum ambient ranges from about 10^{-3} torr to about 10^{-2} torr.

22. (Original) The method as recited in claim 17, wherein a rising rate of the temperature for the heat treatment process ranges from about 3 °C /min to about 25 °C /min.

23. (Original) The method as recited in claim 16, wherein a falling rate of the temperature for the heat treatment process ranges from about 1 °C /min to about 20 °C /min.

COMMENTS

Reconsideration and allowance in view of the following amendments and the following remarks are respectfully requested.

Claim 1, 14 and 15 are currently amended. No new matter has been added into claims. Support for the currently amended claims may be found throughout the specification as originally filed.

Claims 14 is rejected under 35 U.S.C. §102(e) as being anticipated by Wu (U.S.Pat.6,455,383).

Wu discloses using a rapid thermal annealing (RTA) after depositing a silicon nitride layer 312a in order to redistribute the implanted doping impurities. However, Wu does not teach or suggest heat treatment in an LPCVD furnace for releasing thermal stress exerted during the selective oxidation process and gate sealing nitride layer deposition process as disclosed and claimed by Applicant. As described in an AAPA of the present specification, thermal stress is inevitable after selective oxidation and gate sealing nitride deposition employing the RTA or RTP technique (See page 4, lines 2-6 of the original specification). On the contrary, the present invention employs the LPCVD heat treatment in order to overcome the above problem which results when using the RTA or RTP technique of the prior art. Accordingly, since the present invention is not identical or similar to the cited reference of Wu. Applicant believes that the currently amended Claim 14 is novel with respect to the prior art of record and thus is patentable.

Claim 15 is rejected under U.S.C. §103(a) as being anticipated over Wu in view of Quek.

Claim 1 is rejected under U.S.C. §103(a) as being anticipated over Lee in view of Wu.

Claims 2 and 8 are rejected under U.S.C. §103(a) as being anticipated over Lee in view of Wu, and further in view of Eichman.

In response to this rejection, Applicant notes the following:

As to claim 15, Quek discloses a gate oxide 38 grown by RTA, LPCVD or furnace oxidation over the entire surface. But, Quek is focused on a forming process of the gate oxide 38 using the above process, which is different from the present invention. That is, in accordance with the present invention, the LPCVD heat treatment is carried out after a selective oxidation process by means of the RTP, in order to release the stress exerted during the selective oxidation process. Therefore, even if the LPCVD is used in Quek, the purposes of employing the LPCVD in Quek are clearly different from its use in the present invention. Accordingly, Quek fails to make up for the deficiencies of Wu, and thus the combination with Wu also fails to teach or suggest Claim 15, particularly, LPCVD heat treatment for releasing stress exerted during the selective oxidation process and gate sealing nitride layer deposition process.

As to claim 1, Lee discloses a RTP annealing process for changing a WNx layer to a W film which is simultaneously performed for reducing the number of thermal treatment processes. That is, in comparison with the present invention, the RTP annealing process of Lee is carried out differently with respect to the purpose and the performing step. Accordingly, the combination of Lee and Wu fails to teach or suggest that the LPCVD heat treatment process is carried out for releasing stress exerted during the selective oxidation process after carrying out the selective oxidation process. Thus, the combination of Lee and Wu fails to render Claim 1 obvious.

As to Claims 2 and 8, Eichman discloses a method for forming a low resistivity TiN film using TiCl4 and NH3 gases by means of LPCVD under in-situ or under ex-situ. That is, Eichman is focused on the point that after the TiCl4 gas flows into the LPCVD chamber, the NH3 gas flows into the LPCVD chamber for stripping off the remaining unbound chlorine within TiN film,

which may be performed in the same LPCVD chamber or in another LPCVD chamber. Therefore, nowhere does Eichman teach or suggest LPCVD heat treatment and the gate sealing nitride layer formation processes which are carried out under in-situ or ex-situ as disclosed and claimed by Applicant.

Applicant notes with appreciation the allowability of claims 3 – 7, 9 – 13 and 10 – 23. However, Applicant respectfully resubmits that all pending claims, namely 1 – 23, are patentably distinguishable from the cited references for at least the reasons discussed above.

If there are any fees due in connection with the filing of this response, please charge those fees to our Deposit Account No. 02-2666. If a telephone interview would expedite the prosecution of this Application, the Examiner is invited to contact the undersigned at (310) 207-3800.

Respectfully submitted,

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Dated: November 22, 2004

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11/22/04

Linda Marie D'Elia November 22, 2004